VERY LOW POWER GIGABIT LOGIC CIRCUITS WITH ENHANCEMENT-MODE GaAs MESFETS

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ABSTRACT

Ultra high-speed enhancement-mode GaAs MESFET integrated circuits, 0.6 μm in gate length, were fabricated using electron beam direct writing and employing recessed gate structure. The minimum delay time was 28.7 ps per gate with 2.3 mW power dissipation. At liquid nitrogen temperature, 77 K, the delay time was reduced to 17.5 ps with 9.2 mW power dissipation. A divide-by-eight counter was successfully demonstrated at 3.8 GHz with a power consumption of 23.6 mW per chip or 1.2 mW per gate.

Introduction

GaAs digital integrated circuits are receiving increasing attention for ultra high-speed logic application. The 34 ps minimum gate delay has been reported using a depletion-mode BFL[1] and binary frequency dividers have been operated at around 5 GHz up to now[2, 3], though power dissipation of these BFLs was about 40 mW per gate.

However, as the logic circuits become more integrated, the requirement for low power dissipation gate becomes more stringent. For LSI circuit complexity, SDFL[4] and DCFL[5, 6] are promising devices, since their power dissipation is located at 100 μW to 1 mW per gate, approximately. Compared to SDFL, DCFL has the advantages of circuit simplicity, as it requires only one power supply and no level shift diode.

The objective of this paper is to demonstrate the DCFL capability in achieving gigabit logic operations. To improve the speed performance, submicron gate length and recessed gate structure were employed using electron beam lithography.

Inverter Design

Performance for a DCFL gate, consisting of enhancement-mode MESFET driver and resistance load, was numerically analyzed from ring oscillator simulation, applying an equivalent FET circuit model, shown in Fig. 1. In the FET circuit, a Lehovec-Zuleeg model[7] was adopted for the drain current, using following material parameters; electron drift-velocity $v = \mu E/(1 + \mu E/v_s)$, saturation velocity $v_s = 1.5 \times 10^7$ cm s^{-1}, mobility $\mu = 4000$ cm^2 V^{-1} s^{-1} at carrier concentration $n = 1 \times 10^{17}$ cm^{-3}.

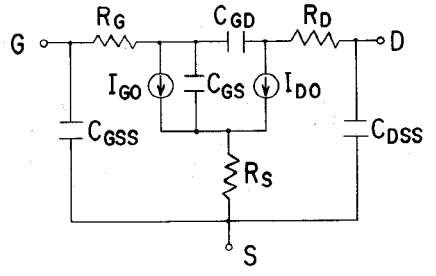
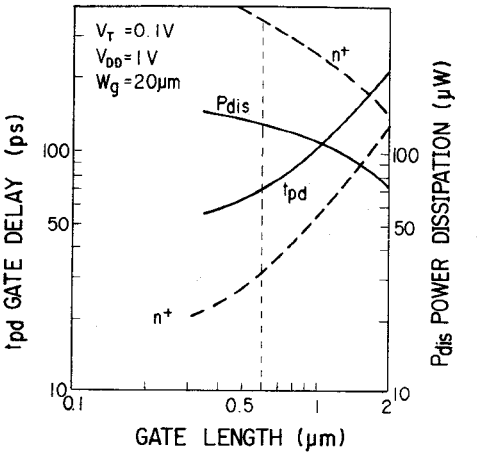
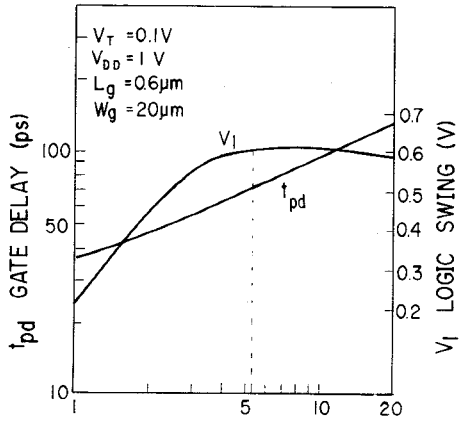


Figure 1. Equivalent FET circuit model.

Figure 2(a) shows gate delay and power dissipation versus gate length under nearly constant logic swing. As the gate length is reduced, the gate delay first decreases rapidly and then tapers off. This results from the fact that series resistance in the FET is composed of a gate length dependent component, channel resistance, and a nondependent component, ohmic contacts. In a small gate length region, the constant resistance becomes the main factor. Therefore, calculated gate delay of 70 ps can be greatly reduced to 32 ps, if the low resistive n^+ layer are introduced at source and drain ohmic regions at 0.6 μm gate length.



(a) Gate delay and power dissipation versus gate length



(b) Gate delay and logic swing versus load resistance

Figure 2. Calculated DCFL gate performance. $L_{GS} = L_{DG} = 2\mu m$, $C_{GSS} = C_{DSS} = 1$ fF.

In Figure 2(b) gate delay and logic swing versus load resistance is shown. As the load resistance becomes large, the logic swing increases due to decrease in low level voltage and then saturates. A load resistance value of 5.3 kΩ, which corresponds to the largest logic swing of 0.6 V, was realized experimentally.

Fabrication Technology

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The IC fabrication technology is similar to those described earlier[6,8]. A sulphur-doped n-type VPE layer grown from an $AsCl_3$ process with an undoped buffer layer on Cr-O doped semi-insulating GaAs substrate was used as an active layer. Its carrier concentration was about 1×10^{17} cm^{-3}. Its thickness was reduced to about 0.15 μm by photo stimulated anodic oxidation.

The fabrication process consists of five masks: an ohmic contact, mesa isolation, a Schottky gate, air-gapped insulation, and interconnection metallization. Electron beam direct writing with a spot-beam system machine was employed for the ohmic and the gate patterns and 1/4 projection photolithography for the others.

Ohmic contacts were formed by evaporating, lifting-off, and alloying AuGe-Ni.

Mesa etching, 0.5 μm deep, for device isolation was accomplished using argon ion milling followed by chemical etching, resulting in a tapered mesa structure capable of preventing gate metal disconnection.

Following the gate pattern delineation using PMMA as EB-resist, the GaAs active layer was chemically etched through the gate stripe to obtain the normally-off condition thickness and a recess structure. The etched depth was about 700 A, which was made longer than surface depletion layer caused by the electron traps. Al-Pt Schottky metals were evaporated and lifted off. First level interconnection metallization was also made at the same time.

Then, air-gapped insulation at interconnection crossover points was prepared by photoresist coating, patterning, and annealing to smooth angles[9].

Finally, second level interconnection metallization was fabricated by evaporating TiAu and defining with ion milling.

Figure 3 shows a fabricated IC chip. The FET gate was 0.6 μm long and 20 μm wide. Source to drain spacing was 4 μm. The load resistance 5.3 kΩ was composed of 20 μm wide and 40 μm long epitaxial n-layer. The unit ICs consisted of monitor inverters, 15-stage ring oscillators with 1/1 and 2/2 fan-in/fan-out, master-slave (8 NOR gates) and T-connected (6 NOR gates) flip-flop binary frequency dividers, and three stage dividers (divide-by-eight counters). The chip was 2.2 mm square.

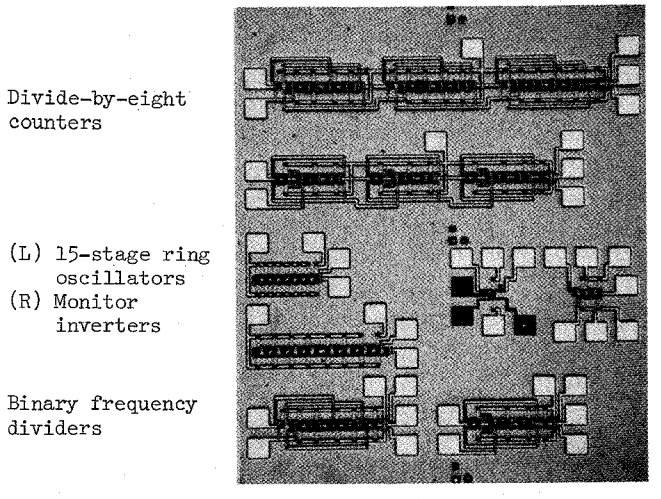


Figure 3. Fabricated unit IC chip.

IC Performance

DC characteristics

Typical DC characteristics for an enhancement-mode MESFET are as follow: Threshold voltage was 0.05 V, drain current was 400 μA and transconductance was 0.9 mS, when gate and drain voltages were 0.6 and 1.0 V, respectively.

Ring Oscillators

Figure 4 shows delay time versus power dissipation relationship as functions of supply voltage V_{DD} and fan-in/fan-out FI/FO, where the solid lines represent experimental values and the broken lines theoretical values. With a 1/1 FI/FO, the measured delay time decreased from 78.3 to 28.7 ps, and the associated power dissipation increased from 52 μW (4.1 fJ) to 2.3 mW (66 fJ), when V_{DD} increased from 0.67 to 4 V. The minimum delay time obtained was smaller than that reported for depletion-mode FETs[1] and the power dissipation was about 20 times smaller. The delay time for FI/FO = 2/2 was 1.5 - 1.7 times larger than that for FI/FO = 1/1. At V_{DD} = 1 V, the delay time was 64 ps for FI/FO = 1/1 and 107 ps for FI/FO = 2/2.

Operation at liquid nitrogen temperature resulted in higher switching speed. At V_{DD} = 4 V, the delay time was 18.4 ps, which corresponds to 64 percent of the room temperature value. The minimum delay time was 17.5 ps with 9.2 mW associated power dissipation at V_{DD} = 5 V. The speed improvement is mainly due to electron mobility increase from about 4000 cm^2 V^{-1} s^{-1} at 300 K to 6000 cm^2 V^{-1} s^{-1} at 77 K for the epitaxial layer doped with 1×10^{17} cm^{-3}.

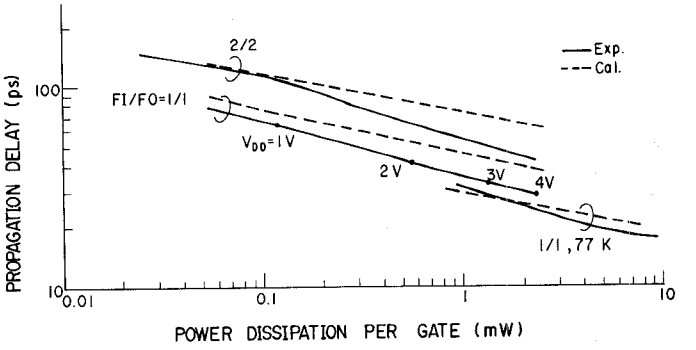


Figure 4. Propagation delay versus power dissipation per gate as functions of supply voltage and fan-in/fan-out.

Frequency Dividers

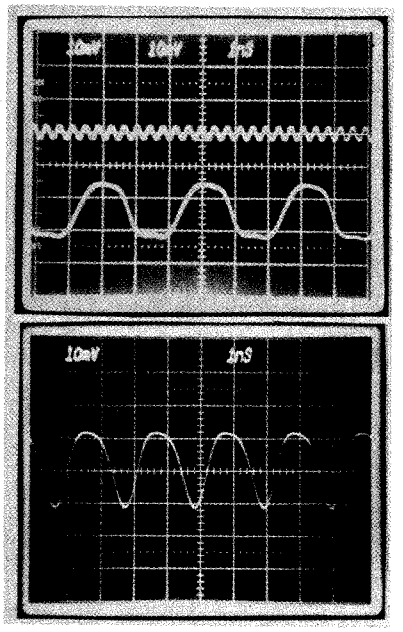
For the master-slave binary divider, the highest input frequency obtained was 2.3 GHz at V_{DD} = 2.6 V. Associated power dissipation including that of output buffer gates was 10.5 mW. Because it employed a built-in inverter for feeding $\bar{C}$ signal to the slave flip-flop, logic analysis indicates that correct operation should be maintained up to 1/5 τd, where τd is an average propagation delay for a NOR gate.

For the T-type binary frequency divider, the maximum clock frequency was typically 2.6 GHz with 6.5 mW power dissipation at V_{DD} = 2.3 V. Theoretically, this kind of frequency divider indicates higher maximum clock frequency 1/4 τd.

Both kinds of divide-by-eight counters were also tested and correct operation was confirmed. The maximum clock frequency for the divide-by-eight counters was almost the same as that of the divide-by-two counters under the same supply voltage.

Figure 5 shows examples of divide-by-eight operation for a T-type counter at different input frequencies of 2.6 GHz at (a) and 3.7 GHz at (b). Only the output waveform is shown in (b), however.

Minimum power dissipation versus input frequency for the divide-by-eight counter is shown in Fig. 6. In order to compare its performance with that for other logic gates, dissipation power is normalized to the value of the binary frequency divider; one-third that of the actual divide-by-eight counter. Divide-by-two operations at 1 GHz with 0.4 mW power consumption, at



(a) f_i = 2.6 GHz
V_{DD} = 2.1 V

(b) f_i = 3.7 GHz
V_{DD} = 3.2 V

Figure 5. Divide-by-eight operation at different clock input frequencies.

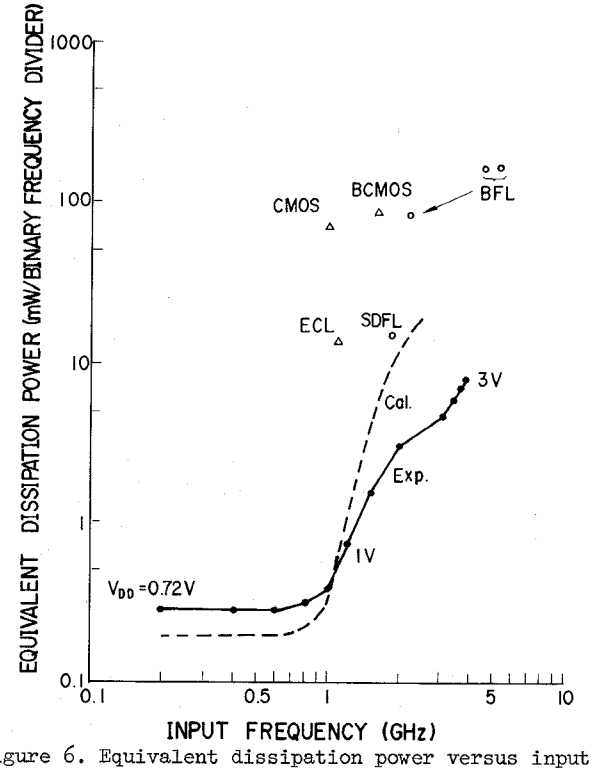


Figure 6. Equivalent dissipation power versus input frequency for the divide-by-eight counter.

2 GHz with 3 mW, and at 3.8 GHz with 8 mW were possible in the present GaAs DCFL. An equivalent gate delay of 66 ps for the 3.8 GHz maximum input frequency shows good coincidence with ring oscillator data 65 ps for FI/FO = 2/2 at V_{DD} = 4 V. The corresponding power dissipation per gate was 1.2 mW, also in agreement with the ring oscillator data.

Typical input voltage was 0.6 V peak-peak superimposed on DC voltage of 0.2 V at 2 GHz input frequency.

Maximum input frequency for the silicon logic is located at about 1.5 GHz and its power dissipation is about 50 times larger than that for the present logic. Though GaAs buffered FET logics have been operated at around 5 GHz up to now, dissipation power is one degree larger than those of the DCFL.

Conclusion

GaAs DCFL has been successfully implemented in very low power gigabit logic circuits.

In ring oscillator evaluation, DCFL gate fabricated with 0.6 μm gate length achieved 28.7 ps minimum delay time with 2.3 mW power dissipation. The minimum power-delay product was 4.1 fJ with 52 μW power dissipation. Delay time improvement was confirmed with cooled operation at liquid nitrogen temperature. The 17.5 ps delay time obtained is the highest speed with semiconductor logic gates and is comparable to that for Josephson logic gates.

High speed performance was demonstrated on frequency dividers. The maximum input frequency for the divide-by-eight counter was 3.8 GHz, which is the best result among enhancement-mode gates. The power dissipation was 23.6 mW per chip and is more than one degree smaller than that for BFL.

Further speed improvement will be attained by realizing n^+ low resistance ohmic layers at the source and drain regions.

The performance reported here encourages the development of DCFL approach for LSI, VLSI range of complexity, where applications to cache memories and gigabit prescalers can be forecasted.

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References

1. P. T. Greiling, C. F. Krumm, F. S. Ozdemir, L. H. Hackett, and R. F. Lohr, Jr., "Electron-beam fabricated GaAs FET inverter," IEEE Trans. Electron Devices, vol. ED-25, pp. 1340, 1978.
2. R. L. Van Tuyl, C. A. Liechti, R. E. Lee, and E. Gowen, "GaAs MESFET logic with 4 GHz clock rate," IEEE J. Solid-State Circuits, vol. SC-12, pp. 485-496, 1977.
3. M. Cathelin, G. Durand, M. Gavant, and M. Rocci, "5 GHz binary frequency division on GaAs," Electron. Lett., vol. 16, pp. 535-536, 1980.
4. R. C. Eden, B. M. Welch, and R. Zucca, "Planar GaAs IC technology: Applications for digital LSI," IEEE J. Solid-State Circuits, vol. SC-13, pp. 419-426, 1978.
5. H. Ishikawa, H. Kusakawa, K. Suyama, and M. Fukuta, "Normally-off type GaAs MESFET for low power, high speed logic circuits," in ISSCC Dig. Tech. Papers, pp. 200-201, 1977.
6. T. Mizutani, M. Ida, and M. Ohmori, "An 80-ps normally-off GaAs MESFET logic," in Proc. First Specialty Conf. Gigabit Logic Microwave Systems (Orland, FL), pp. 93-101, 1979.
7. K. Lehovec and R. Zuleeg, "Voltage-current characteristics of GaAs J-FET's in the hot electron range," Solid-State Electronics, vol. 13, pp. 1415-1426, 1970.
8. N. Kato, T. Mizutani, S. Ishida, and M. Ohmori, "Electron-beam fabrication of submicrometer gates for a MESFET logic," IEEE Trans. Electron Devices, vol. ED-27, pp. 1098-1101, 1980.
9. M. Ida, M. Uchida, K. Shimada, H. Sakamoto, K. Asai, and S. Ishida, "Bridged leads power FET," Rep. Electron Devices, IECE Japan ED 78-86, 1978 (in Japanese).